



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

| APPLICATION NO.   | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.       | CONFIRMATION NO. |
|---|-------------|----------------------|---------------------------|------------------|
| 10/604,059  | 06/24/2003  | Charles N. Perez     | BUR920030032US1           | 1058             |
| 28211 7590 01/08/2007<br>FREDERICK W. GIBB, III<br>GIBB INTELLECTUAL PROPERTY LAW FIRM, LLC<br>2568-A RIVA ROAD<br>SUITE 304<br>ANNAPOLIS, MD 21401 |             |                      | EXAMINER<br>DOAN, NGHIA M |                  |
|   |             |                      | ART UNIT<br>2825          | PAPER NUMBER     |
| SHORTENED STATUTORY PERIOD OF RESPONSE  |             | MAIL DATE            | DELIVERY MODE             |                  |
| 3 MONTHS  |             | 01/08/2007           | PAPER                     |                  |

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

## Office Action Summary

Application No.

10/604,059

Applicant(s)

PEREZ ET AL.

Examiner

Nghia M. Doan

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 10/05/2006 and RCE 11/16/2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1, 5, 13, 17, 25, 29-30, 33, 35-36, 38-39, 42, and 44 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 5, 13, 17, 25, 29-30, 33, 35-36, 38-39, 42, and 44 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/05/2006 has been entered.
2. The claims 1, 5, 13, 17, 25, 29-30, 33, 35-36, 38-39, 42, and 44 remain pending. Claims 1, 5, 13, 25, 29, and 30 have been amended. Claims 2-4, 6-12, 14-16, 18-24, 26-28, 31-32, 34, 37, 40, 41, and 43 have been canceled.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 5, 13, 17, 25, and 29-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Ker et al. (hereinafter as "Ker"), *Automatic methodology for placing the guard rings into chip layout to prevent latchup in CMOS IC's*, IEEE, Vol. 1, September 2001, Pages 113-116.
5. With respect to claims 1, 13, and 25, Ker discloses a computer storage device readable by machine, tangibly embodying a program of instructions executable by the

Art Unit: 2825

machine to perform a method of displaying a guard ring within (hierarchical) *(the double guard rings are often used to surround the output PMOS and NMOS in I/O cells ... the additional guard rings should be placed between the I/O cells and the Internal circuits.)*(Page 113, col. 2, paragraph 3 and figures 3 and 4(b)) an integrated circuit design having logic devices (*"Guard Ring Automation" program to realize the additional guard rings in the layout is proposed to make the layout more automatically and accurately*)(The Abstract, page 113), said method comprising:

determining positions of said logic devices within *(claim 13, a portion of said hierarchical)* said integrated circuit design *(the location to be added the additional guard rings (figure 5, Page 115, col. 1, paragraph 2; the signal lines such as a, b, c, d, e, and f pass through the region where to be added the guard ring (figure6, page 115, paragraphs 1 and 2); and the double guard rings are often used to surround the output PMOS and NMOS in I/O cells ... the additional guard rings should be placed between the I/O cells and the Internal circuits.)*(page 113, col. 2, paragraph 3);

incorporating *(forming/adding)* said guard ring into *(claim 13, said portion of said hierarchical)* said integrated circuit design *(automatically place the guard ring in the chip layout to improve latchup immunity of the CMOS IC's (the Abstract); Guard rings are formed by the p+ diffusions in the p-substrate connect to VSS and the n+ diffusions in the n-well connect to VDD. To effectively absorb the trigger current in the well or substrate, the contacts for connection to guard rings should be added as many as possible, (Page 114, Section 2. Guard Rings Automation) and figures 5 and 6 show the guard rings before and after added); and*

displaying (*claim 13, said portion of*) said logic devices and guard ring symbolically (*figs 3 through fig. 8*) and schematically (*figs 3 through fig. 8*) in a single display (*the instance show in Fig. 4(a) and 4(b) are displayed in the master layout views. To simplify the display in the top-level design....*)(page 114, section 2.1 Instance and Mosaic, figure 4 descriptions), wherein said displaying of said logic devices and said guard ring symbolically comprises displaying a parameterized symbol (*figure 4 and its description as page 114-115*) comprising displaying parameters including at least one of a type of said guard ring (*n-type and p-type of guard rings*)(*figure 4 and its description as page 114-115*) and an efficiency of said guard ring (*the program will use instance to get the most area efficiency in the guard ring placement. Thus, the proposed Guard Ring Automation program gets a balance between the speed and the are efficiency to add the additional guard rings for latchup prevention*)(*type of guard rings such as p-diffusion ring and n-diffusion ring; dimension of guard ring such as D horizontal= the width of guard ring region, D vertical= the height of guard ring region; placement depending on the shape of guard ring such as non-rectangle shape use the instance to add the guard ring and rectangle shape use mosaic to add the guard ring; the electrical connection of guard ring such as p+ diffusions in the p-substrate connect to VSS and the n+ diffusions in the n-well connect to VDD*) (pages 114-115 and figures 3-6 and 8).

6. With respect to claims 30 and 39, Ker discloses all the limitations in set forth claims, further comprising displaying said logic devices and said guard ring graphically in said single display (*pages 114-116 and figures 3-6 and 8*).

7. With respect to claims 5, 17, and 29, Ker discloses all the limitations in set forth claims wherein said displaying of said logic devices displays and said guard ring graphically comprise illustrating relative position of said logic device and guard ring (*W instance and H instance; D horizontal and D vertical*) (*figures 4 and 5 and their descriptions; and pages 114-115*).

8. With respect to claims 33, 35-36, 38, 42, and 44, Ker discloses all the limitations in set forth claims, wherein said displaying of said parameterized symbol comprises displaying said parameters including (*as per claims 33, 35-36, 38, 42, and 44*) a type of circuit (*p-substrate/n-well, I/O circuit and internal circuit*) and (*as per claims 35, 38, and 44*) an efficiency of said guard ring (*the program will use instance to get the most area efficiency in the guard ring placement. Thus, the proposed Guard Ring Automation program gets a balance between the speed and the are efficiency to add the additional guard rings for latchup prevention*) (*type of guard rings such as p-diffusion ring and n-diffusion ring; dimension of guard ring such as D horizontal= the width of guard ring region, D vertical= the height of guard ring region; placement depending on the shape of guard ring such as non-rectangle shape use the instance to add the guard ring and rectangle shape use mosaic to add the guard ring; the electrical connection of guard ring such as p+ diffusions in the p-substrate connect to VSS and the n+ diffusions in the n-well connect to VDD*) (*pages 114-115 and figures 3-6 and 8*).

Art Unit: 2825

**Examiner Remarks**

9. Acknowledgment is made of Applicant's arguments filed on 10/05/2006, Applicant is/are invited to review the claim rejection above, which is address all the claim limitations in detailed and it also resolves all the issues per applicant arguments.

**Conclusion**

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

 Examiner

N. Doan

PAUL DINH  
PRIMARY EXAMINER

